



**PRODUCT/PROCESS
CHANGE NOTIFICATION**

PCN APM-IPC/11/6178
Notification Date 01/11/2011

Linear VReg and VRef BU HBIP40 Technology for Voltage Reference TL431

Table 1. Change Implementation Schedule

Forecasted implementation date for change	04-Apr-2011
Forecasted availability date of samples for customer	04-Jan-2011
Forecasted date for STMicroelectronics change Qualification Plan results availability	04-Jan-2011
Estimated date of changed product first shipment	12-Apr-2011

Table 2. Change Identification

Product Identification (Product Family/Commercial Product)	See attached list
Type of change	Product design change
Reason for change	improve service to ST Customers
Description of the change	Following Divisional Commitments towards a continuous improvement philosophy, a more fine geometry Bipolar Technology called HBIP40 has been qualified in ST. The present PCN notifies the fully qualification of TL431 device, redesigned in the new technology. Unchanged quality standards and electrical performances are guaranteed. Qualification samples of TL431IDT and TL431ACZ are already available for delivery, while the other part numbers in the reference list will be made available on request.
Product Line(s) and/or Part Number(s)	See attached
Description of the Qualification Plan	See attached
Change Product Identification	Digit "H" is marked on the physical parts, on the string after P/N marking
Manufacturing Location(s)	

Table 3. List of Attachments

Customer Part numbers list	
Qualification Plan results	



Customer Acknowledgement of Receipt		PCN APM-IPC/11/6178
Please sign and return to STMicroelectronics Sales Office		Notification Date 01/11/2011
<input type="checkbox"/> Qualification Plan Denied	Name:	
<input type="checkbox"/> Qualification Plan Approved	Title:	
<input type="checkbox"/> Change Denied	Company:	
<input type="checkbox"/> Change Approved	Date:	
	Signature:	
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DOCUMENT APPROVAL

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WHAT:

Following Divisional Commitments towards a continuous improvement philosophy, a more fine geometry Bipolar Technology called HBIP40 has been qualified in ST. The present PCN notifies the fully qualification of TL431 device, redesigned in the new technology.

Unchanged quality standards and electrical performances are guaranteed.

Qualification samples of TL431IDT and TL431ACZ are already available for delivery, while the other part numbers in the reference list will be made available on request.

WHY:

New equipment utilization, capacity optimization.

This manufacturing change will improve service to ST Customers.

HOW:

The qualification program mainly consists of reliability tests and comparative electrical characterizations.

The related reliability report is annexed to this document.

The changes here reported do not affect the electrical, dimensional and thermal parameters of the products, keeping unchanged all information reported on the relevant datasheets.

WHEN:

The implementation will be finalized within Week 12-11

Marking and traceability:

Digit "H" is marked on the physical parts, on the string after P/N marking.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all information reported on the relevant datasheets.

There is as well no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).

In any case, first shipments may start earlier with customer's written agreement.



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Quality and Reliability

Reliability Report

Voltage References

New Products

**TL431IDT - TL431ACZ
TL431AIL3T-TL431AIL5T**

(0431AB6 line)

**Technology HBIP40V
Packages: SO8, TO92, SOT23-3L-5L**

General Information		Locations	
Product Line	0431AB6	Wafer fab	AMK6
Product Description	Programmable voltage reference	Assembly plant	SO8 (BOUSKOURA) TO92 (ASE WEIHAI) SOT23-3L-5L (CARSEM)
P/N	TL431IDT TL431ACZ TL431AIL3T-TL431AIL5T	Reliability Lab	CATANIA
Product Group	IMS-APM- IPC	Reliability assessment	Pass
Product division	Linear Voltage Regulators & Vref		
Packages	SO8, TO92, SOT23-3L-5L		
Silicon Process technology	HBIP40V		
Production mask set rev.	0431H Rev A		

DOCUMENT INFORMATION

Version	Date	Pages	Prepared by	Approved by	Comment
1.0	19-Nov-2010	12	Giuseppe Failla Angelo Basile	Giovanni Presti	Final report

Note: This report is a summary of the reliability trials performed in good faith by STMicroelectronics in order to evaluate the potential reliability risks during the product life using a set of defined test methods.

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1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
JESD47	Stress-Test-Driven Qualification of Integrated Circuits
AEC-Q100	Stress test qualification for automotive grade integrated circuits

2 GLOSSARY

DUT	Device Under Test
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

New products qualification: TL431IDT, TL431ACZ, TL431AIL3T, TL431AIL5T

3.2 Conclusion

Qualification Plan requirements have been fulfilled without exception. It is stressed that reliability tests have shown that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests demonstrates the ruggedness of the products and safe operation, which is consequently expected during their lifetime.


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4 DEVICE CHARACTERISTICS

4.1 Device description

The TL431 is a programmable shunt voltage reference with guaranteed temperature stability over the entire operating temperature range. The device's temperature range is extended for the automotive version from -40°C up to +125°C. The output voltage can be set to any value between 2.5 and 36 V with two external resistors. The TL431 operates with a wide current range from 1 to 100 mA with a typical dynamic impedance of 0.22 Ω.

4.2 Construction note

	P/N			
	TL431IDT	TL431ACZ	TL431AIL3T	TL431AIL5T
Wafer/Die fab. information	SO8	TO92	SOT23-3L	SOT23-5L
Wafer fab manufacturing location	AMK6			
Technology	HBIP40V			
Die finishing back side	Lapped Silicon			
Die size	900 x610um			
Passivation type	PVAPOX/NITRIDE			
Wafer Testing (EWS) information				
Electrical testing manufacturing location	TPY			
Tester	ASL1000			
Test program	T0431CW1			
Assembly information				
Assembly site	BOUSKOURA	ASE WEIHAI	CARSEM	
Package description	SO8	TO92	SOT23-3L	SOT23-5L
Molding compound	NITTO MP8000CH4-2A	Samsung SG-8100G	CEL8240HF10LXC	
Frame material	SO8L 94x125 NRS BTW 4+2+2 NiPdAu	WSD-0250 TO237	HDLF SOT23-3L- COPPER/Ag spot 0.64x0.038	HDLF SOT23-5L- COPPER/Ag spot 0.63x0.039
Die attach process	GLUE			
Die attach material	HITACHI EN4900 ST10	AMICON C990J ABLESTICK	QMI519	
Wire bonding process	Ball on pads, stick on leads			
Wires bonding materials/diameters	0.8 mils Au	1 mils Au	1 mils Au	
Lead finishing process	Plating	Plating	Plating	
Lead finishing/bump solder material	100% Tin Plate	100% Tin Plate	100% Tin Plate	
Final testing information				
Testing location	BOUSKOURA	ASE WEIHAI	CARSEM	
Tester	ASL1000	AZ400S	ASL 1000	
Test program	T0431BF5.PRG	W0431AF4	T0431BF5.PRG	



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5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Diffusion Lot	Assy Lot	Process/ Package	Product Line	Comments
1	60197XV	CZ02709MZZ	SO8	0431AB6	
2	60197XV	GE033146	TO92	0431AB6	
3	60197XV	9Y028XAX	SOT23-3L	0431AB6	
4	60197XV	9Y027WMM	SOT23-5L	0431AB6	

5.2 Test plan and results summary

P/N TL431IDT

Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS				Note
						SO8	TO92	SOT23-3L	SOT23-5L	
Die Oriented Tests										
HTOL	N	JESD22 A-108	Tj = 125°C, BIAS	77	Bias	+5V	+5V	+7V	+7V	
					168 H	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	0/77	0/77	
HTSL	N	JESD22 A-103	Ta = 150°C	45	168 H	0/45	0/45	0/45	0/45	
					500 H	0/45	0/45	0/45	0/45	
					1000 H	0/45	0/45	0/45	0/45	
Package Oriented Tests										
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Oven Reflow @ Tpeak=260°C 3 times	231	Final	Pass	NO PC has been performed	Pass	Pass	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C	77	96 H					
					168 H	0/77	0/77	0/77	0/77	
TC	Y	JESD22 A-104	Ta = -65°C to 150°C	77	100 cy	0/77	0/77	0/77	0/77	
					200 cy	0/77	0/77	0/77	0/77	
					500 cy	0/77	0/77	0/77	0/77	
THB	Y	JESD22 A-101	Ta = 85°C, RH=85%, BIAS	77	Bias	+3V	+3V	+3V	+3V	
					168 H	0/77	0/77	0/77	0/77	
					500 H	0/77	0/77	0/77	0/77	
					1000 H	0/77	0/77	Note 1	0/77	

Note 1: The data related to 1000h are extrapolated from SOT23-5L



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6 ANNEXES

6.1 Device details

6.1.1 Pin connection

Figure 1. TO-92 pin connections (top view)

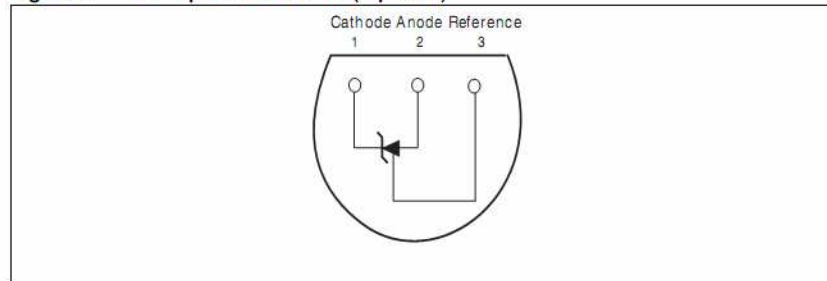


Figure 2. SO-8 batwing pin connections (top view)

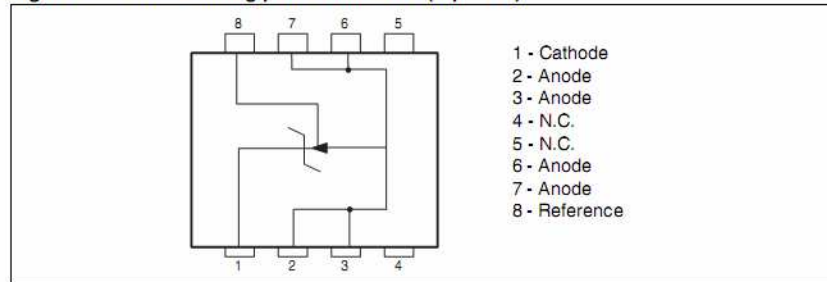
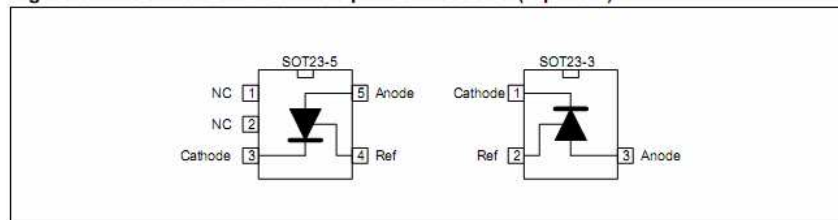
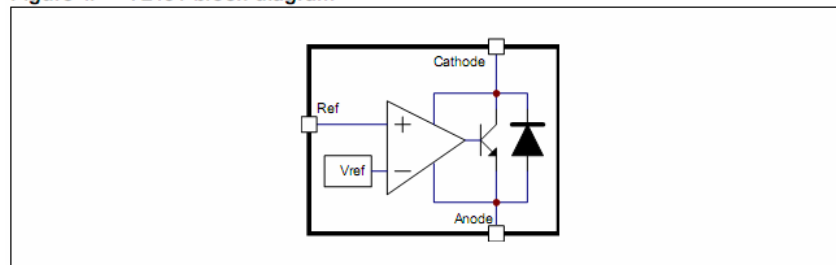


Figure 3. SOT23-5 and SOT23-3 pin connections (top view)



6.1.2 Block diagram

Figure 4. TL431 block diagram

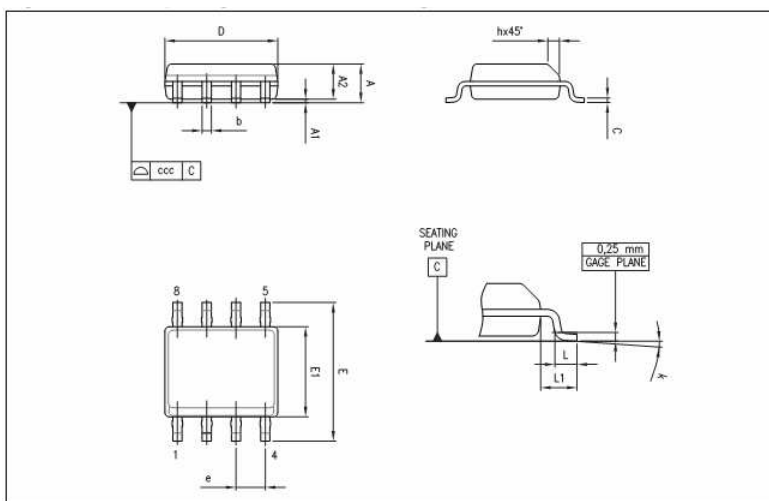




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6.1.3 Package outline/Mechanical data

SO-8 package information

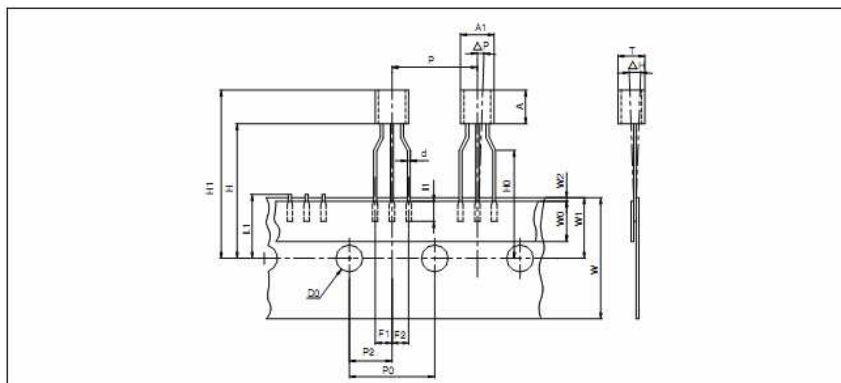


Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.069
A1	0.10		0.25	0.004		0.010
A2	1.25			0.049		
b	0.28		0.48	0.011		0.019
c	0.17		0.23	0.007		0.010
D	4.80	4.90	5.00	0.189	0.193	0.197
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e		1.27			0.050	
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
L1		1.04			0.040	
k	1°		8°	1°		8°
ccc			0.10			0.004



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TO-92 ammpack and tape and reel package information

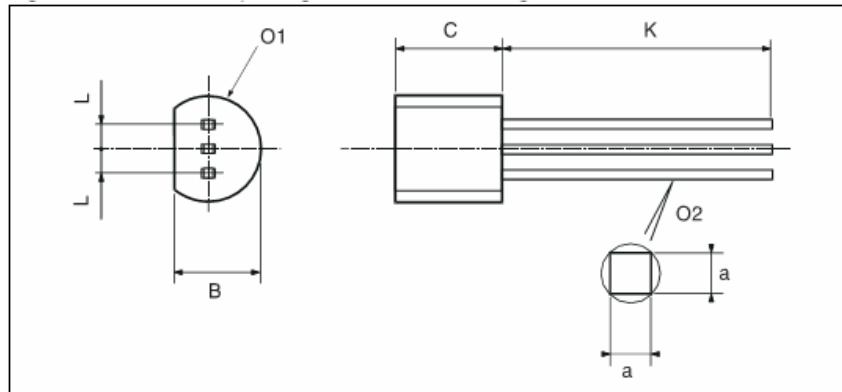


Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
AL			5.0			0.197
A			5.0			0.197
T			4.0			0.157
d		0.45			0.018	
l1	2.5			0.098		
P	11.7	12.7	13.7	0.461	0.500	0.539
PO	12.4	12.7	13	0.488	0.500	0.512
P2	5.95	6.35	6.75	0.234	0.250	0.266
F1/F2	2.4	2.5	2.8	0.094	0.098	0.110
Δh	-1	0	1	-0.039	0	0.039
ΔP	-1	0	1	-0.039	0	0.039
W	17.5	18.0	19.0	0.689	0.709	0.748
W0	5.7	6	6.3	0.224	0.236	0.248
W1	8.5	9	9.75	0.335	0.354	0.384
W2			0.5			0.020
H			20			0.787
H0	15.5	16	16.5	0.610	0.630	0.650
H1			25			0.984
DO	3.8	4.0	4.2	0.150	0.157	0.165
L1			11			0.433



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TO-92 (bulk) package information

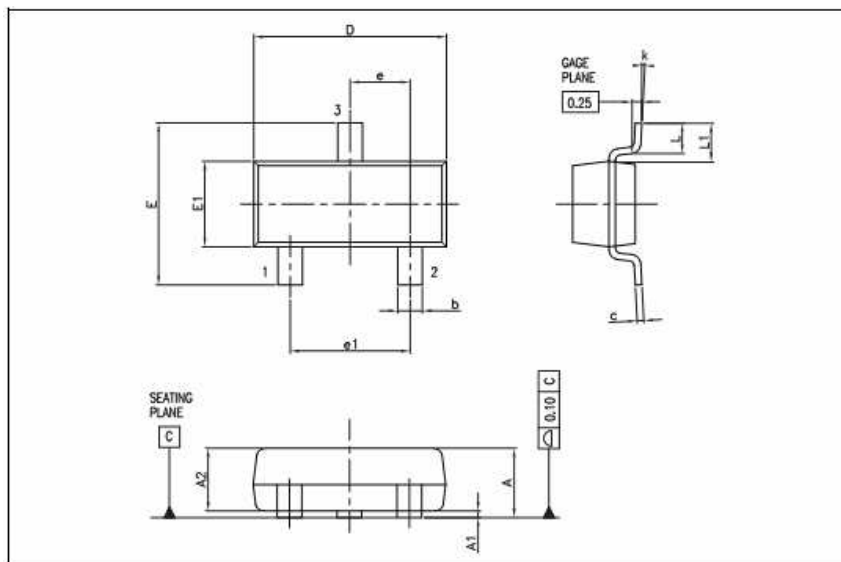


Dim.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
L		1.27			0.05	
B	3.2	3.7	4.2	0.126	0.1457	0.1654
O1	4.45	5.00	5.2	0.1752	0.1969	0.2047
C	4.58	5.03	5.33	0.1803	0.198	0.2098
K	12.7			0.5		
O2	0.407	0.5	0.508	0.016	0.0197	0.02
a	0.35			0.0138		



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SOT23-3 package information

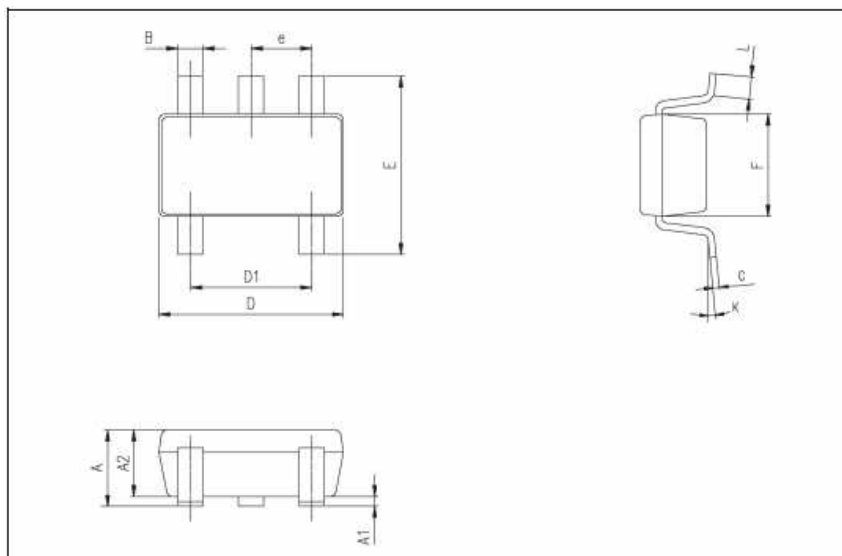


Dimensions						
Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.89		1.12	0.035		0.044
A1	0.01		0.10	0.0004		0.004
A2	0.88	0.95	1.02	0.035	0.037	0.040
b	0.30		0.50	0.012		0.020
c	0.08		0.20	0.003		0.008
D	2.80	2.90	3.04	0.110	0.114	0.120
E	2.10		2.64	0.083		0.104
E1	1.20	1.30	1.40	0.047	0.051	0.055
e		0.95			0.037	
e1		1.90			0.075	
L	0.40	0.50	0.60	0.016	0.020	0.024
L1		0.54			0.021	
k	0d		8d			



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SOT23-5 package information



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.90	1.20	1.45	0.035	0.047	0.057
A1			0.15			0.006
A2	0.90	1.05	1.30	0.035	0.041	0.051
B	0.35	0.40	0.50	0.013	0.015	0.019
C	0.09	0.15	0.20	0.003	0.006	0.008
D	2.80	2.90	3.00	0.110	0.114	0.118
D1		1.90			0.075	
e		0.95			0.037	
E	2.60	2.80	3.00	0.102	0.110	0.118
F	1.50	1.60	1.75	0.059	0.063	0.069
L	0.10	0.35	0.60	0.004	0.013	0.023
K	0 degrees		10 degrees			



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6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operative Life	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.

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